ABSTRACT

Whether an initial command outputted from a host
is 'CMD1' or 'CMD55+CMD41' is detected with an initial
command detection portion 8, and the result of
detection is set in an SD/MMC register 13. Reset
process for hardware and that for firmware are carried
out based on the result of detection set in the SD/MMC
register 13. Thereafter, a microcomputer 7 sets data
indicating in which mode, MultiMedia Card mode or SD
mode, the firmware reset process was carried out, in
a F/W process SD/MMC register 14. A H/W-F/W mode
comparison circuit 15 compares data in the SD/MMC
register 13 with data in the F/W process SD/MMC
register 14. If these data agree with each other,
busy state is released, and command wait state is
established. If they disagree with each other, a
disagreement occurrence detection signal is
outputted to the microcomputer 7, and power-on reset
processing is performed again.